



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,399	10/08/2003	Yuanning Chen	TI-35212	7440
23494	7590	11/29/2005	EXAMINER	
TEXAS INSTRUMENTS INCORPORATED			FARAHANI, DANA	
P O BOX 655474, M/S 3999			ART UNIT	
DALLAS, TX 75265			PAPER NUMBER	
			2891	

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/681,399

Applicant(s)

CHEN ET AL.

Examiner

Dana Farahani

Art Unit

2891

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 02 September 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-19 and 24-27 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-19 and 24-27 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)             | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

**DETAILED ACTION**

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 24 and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim (US Patent Application Publication 2004/0033647), newly cited.

Regarding claim 1, Kim discloses in figures 2-4, a method of fabricating a semiconductor device, the method comprising:

forming a gate 3a on a semiconductor substrate, the gate including opposing side surfaces;

depositing an oxide material 5 over the gate electrode and the semiconductor substrate, the opposing side surfaces of the gate being substantially free of the oxide material (paragraphs 18 and 19); and

forming spacers 9 on the opposing side surfaces of the gate, the spacers contacting the opposing side surfaces of the gate substantially along the opposing side surfaces.

Regarding claim 2, see paragraph 15, wherein it is stated that the gate is doped.

Regarding claim 3, see paragraph 21 and figure 4, wherein it is shown that sidewall spacers mitigating diffusion of dopants from the opposing surfaces of the gate.

Regarding claims 24 and 25, conductive layer 3 is formed and patterned, over the substrate; and an oxide 5 is deposited on the gate and the substrate.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim as applied to claim 1 above, and further in view of Hong et al., hereinafter Hong (US Patent 5,457,061), previously cited.

Kim discloses the limitations in these claims, as discussed above, except for the oxide material comprising one of the materials mentioned in claim 7, including SiO<sub>2</sub>.

Hong discloses a gate oxide 36 being SiO<sub>2</sub> (see figure 4; and column 3, lines 42-45). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use SiO<sub>2</sub> as the oxide layer of the Kim reference, since it is well known and widely used as an insulator in chip manufacturing.

5. Claims 8-13, 16-19 and 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hong in view of Kim.

Regarding claims 8, 12, 13, 16, 26 and 27, Hong discloses in figures 3-6, a method of fabricating a semiconductor device, the method comprising:

forming a gate 38 on a semiconductor substrate, the gate including opposing side

Art Unit: 2891

surfaces (figure 4),

depositing an oxide material ( $\text{SiO}_2$ ) 36 over the gate electrode and the semiconductor substrate, the opposing side surfaces of the gate being substantially free of the oxide material (see column 3, lines 54-64);

forming spacers 40 on the opposing side surfaces of the gate, the spacers contacting the opposing side surfaces of the gate substantially along the opposing side surfaces (figure 3, and column 4, lines 1-10), and

providing a nitride layer over the gate after depositing the oxide material; and etching the nitride layer (see column 4, lines 1-10).

Hong does not disclose depositing an oxide material over the gate.

Kim discloses this limitation, as discussed above. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use this method to deposit the oxide 36 of the Hong structure as an alternative process to that of the Hong reference, according to one of ordinary skill in the art preference to use the method.

Regarding claims 9, 10, and 18, Hong in view of Kim discloses the limitations in these claims, as discussed above, but does not disclose the LDD regions are formed after forming the gate but before depositing the oxide layer. It would have been obvious to one of ordinary skill in the art at the time of the invention to determine the order of forming these regions, according to the manufacturing environment and convenience of one of ordinary skill in the art. See *Ex Parte Rubin* 126 USPQ 440 (BAP1 1959) for the proposition that reversing the order of a process sequence cannot be considered an act of invention.

Regarding claim 17, Hong discloses the limitations in the claim, as discussed above, except for a p-doped gate. Kim discloses a p-doped gate, as discussed above. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the gate of the Hong reference as p-doped, since it is well known, and is customary in the art to make a doped gate region, since its resistivity can be controlled easily.

Regarding claims 11 and 19, Hong in view of Kim discloses the limitations in the claims, as discussed above, but does not expressly disclose the MOS transistor is PMOS. It would have been obvious to one of ordinary skill in the art at the time of the invention to make the transistor as PMOS according to one of ordinary skill in the art preference of having holes or electrons as the majority carriers.

6. Claims 4-6, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim, and Hong in view of Kim, in case of claims 14 and 15, as applied to claims 1 and 12 above, and further in view of Jeng (US Patent 6,303,490), previously cited.

Kim, and Hong in view of Kim disclose the claimed invention, as discussed above, except for an anisotropic Physical Vapor Deposition (PVD) which comprises one of collimated sputtering, long throw sputtering or ionized metal plasma method is used in depositing the oxide material.

Jeng discloses anisotropic ionized metal plasma sputtering method is used for deposition which gives a good surface coverage (see column 4, lines 24-28). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use this method to deposit the oxide layer of the Kim reference, since the advantages of using the method, such as the advantage mentioned above is well known in the art.

***Response to Arguments***

7. Applicant's arguments with respect to the previously rejected claims have been considered but are moot in view of the new grounds of rejection.


***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (571)272-1706. The examiner can normally be reached on M-F 9:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571)272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D. Farahani

  
**B. WILLIAM BAUMEISTER**  
**SUPERVISORY PATENT EXAMINER**